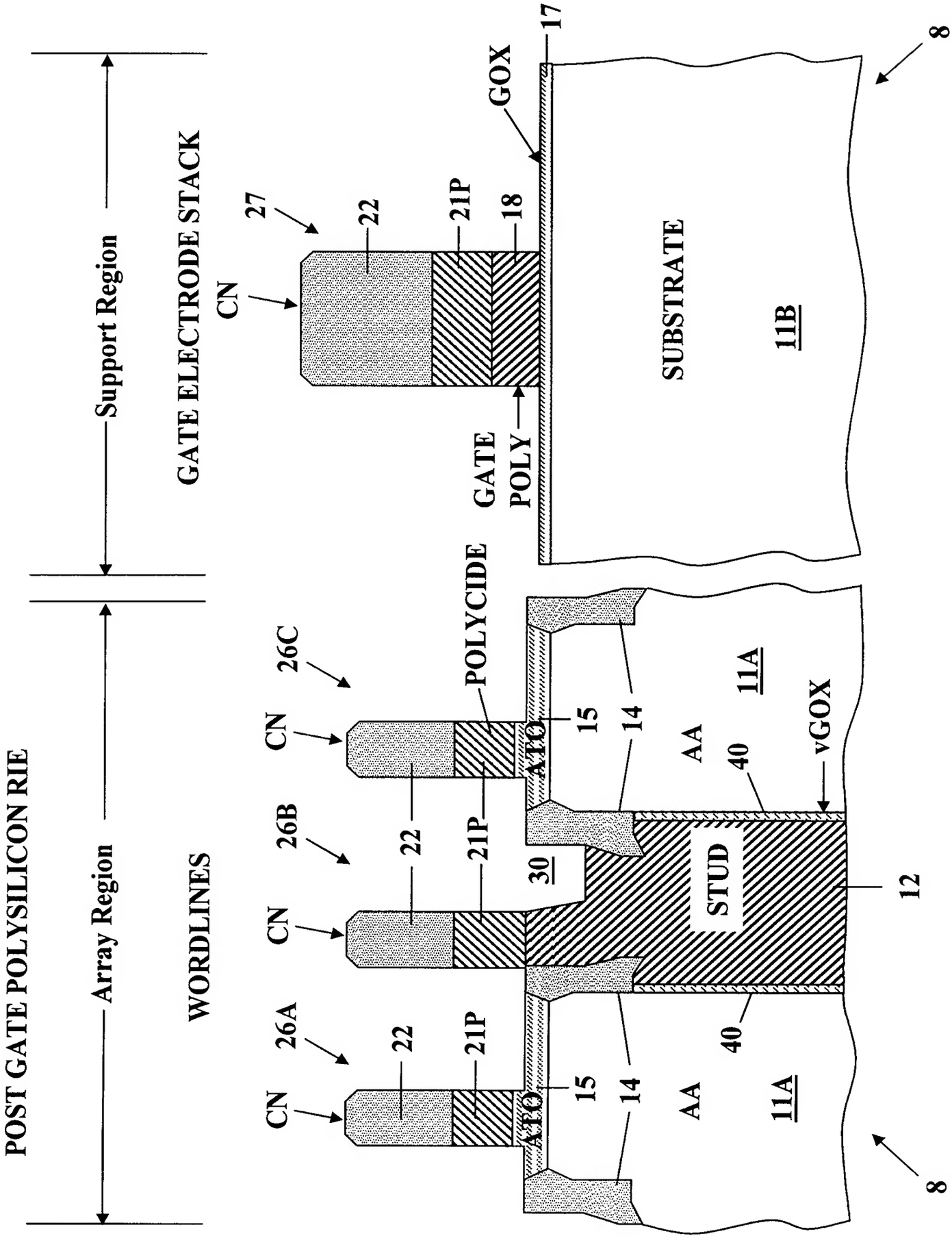
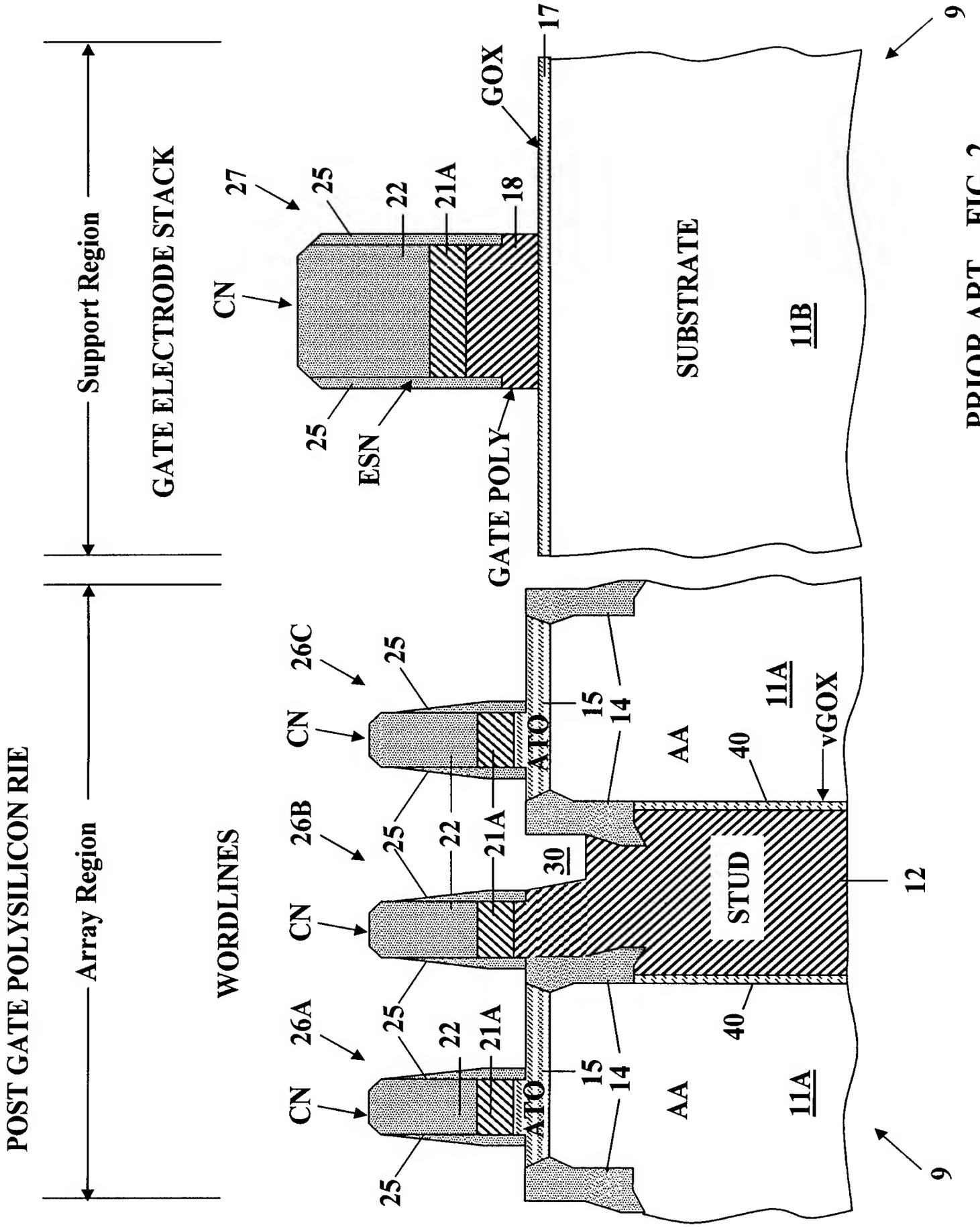


PRIOR ART FIG. 1



PRIOR ART FIG. 2

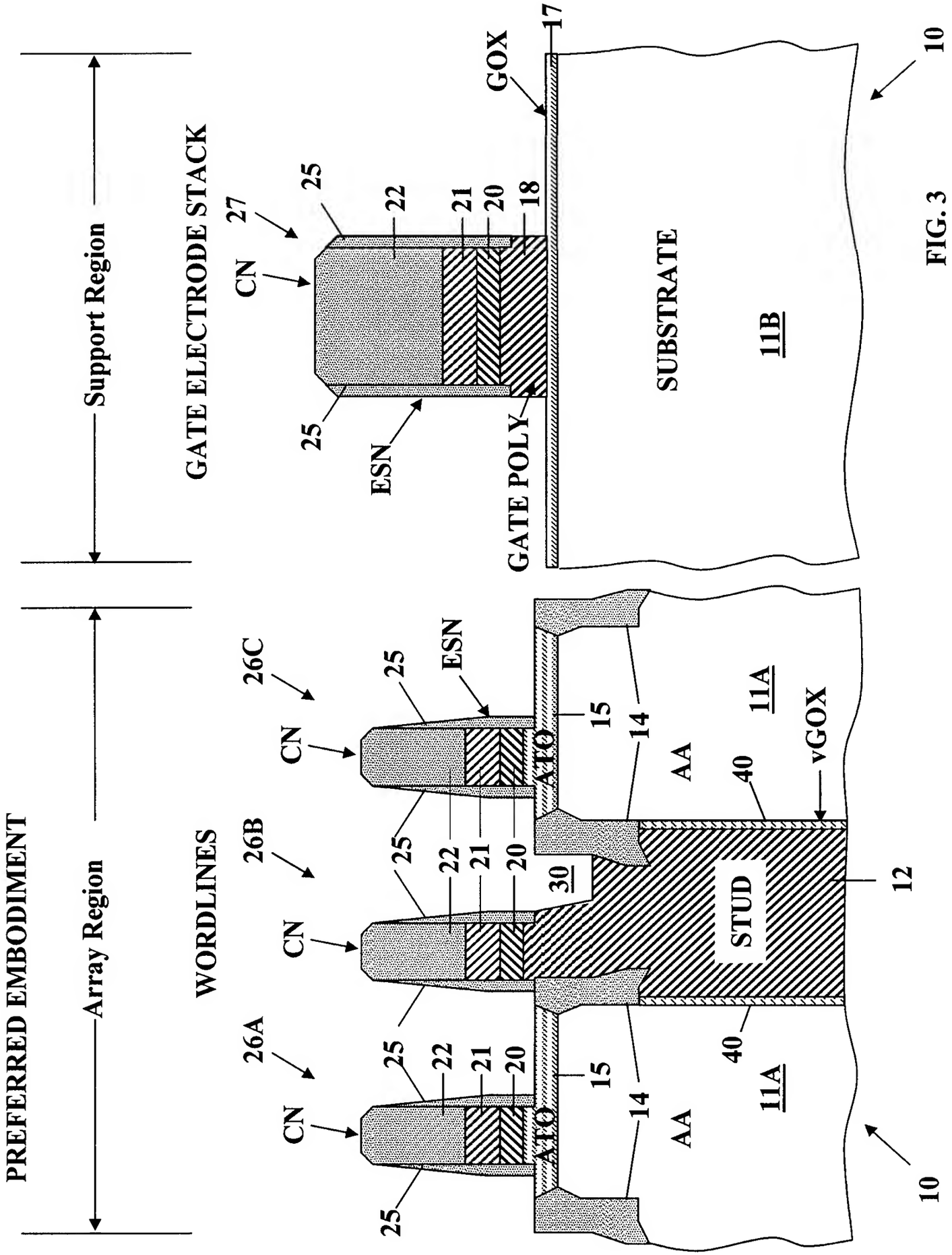
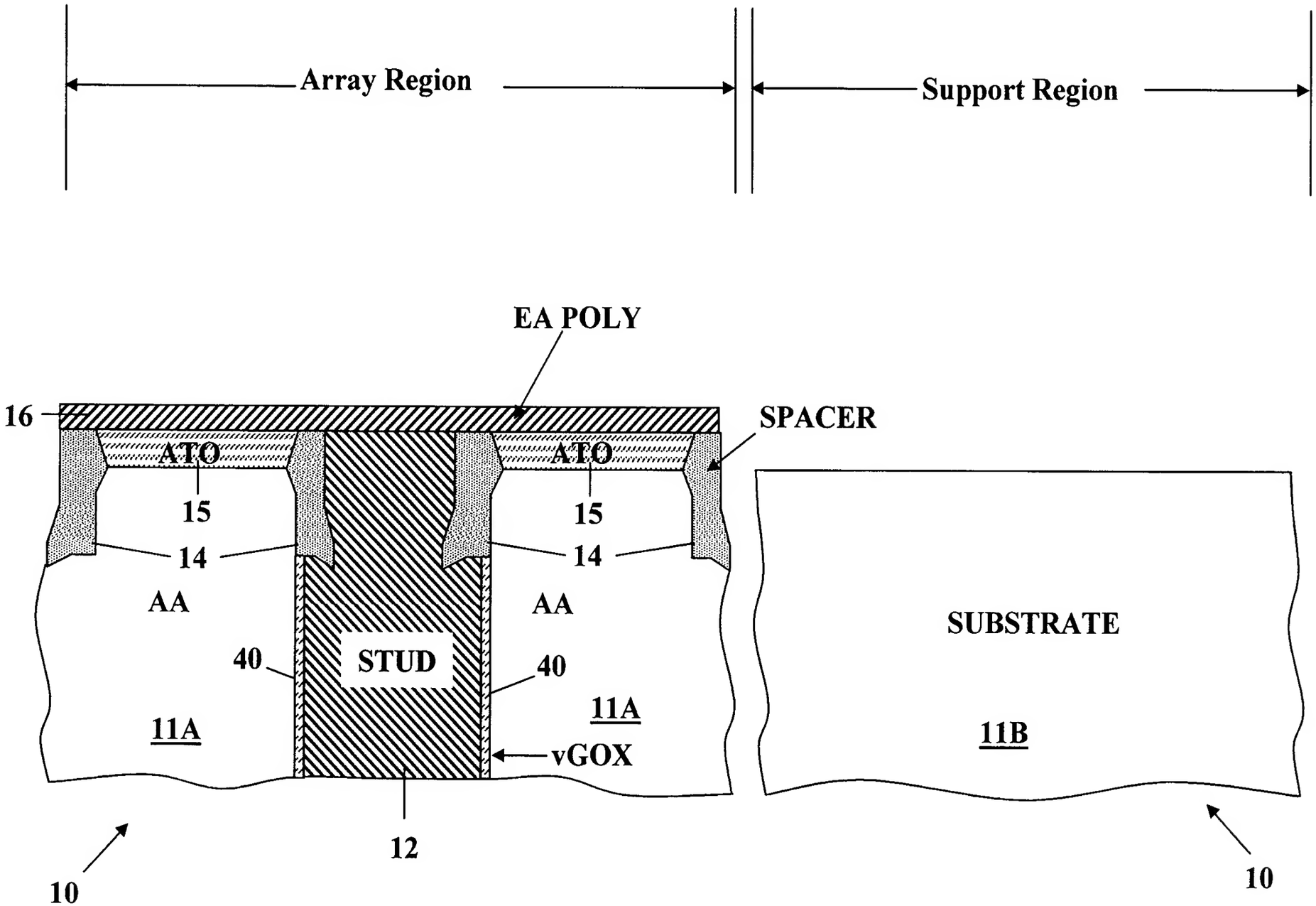

PREFERRED EMBODIMENT
Array Region
Support Region
WORDLINES
GATE ELECTRODE STACK
26A
26B
26C
CN
25
22
21
20
18
27
ESN
GATE POLY
GOX
17
SUBSTRATE
11B
11A
AA
ATO
15
14
30
STUD
12
40
vGOX
10

FIG. 3

1. TOE (TOP OXIDE EARLY) PROCESS FOR ATO (ARRAY REGION TOP OXIDE)



• Post ES/EA process(prior art)

FIG. 4

2. GATE OXIDATION

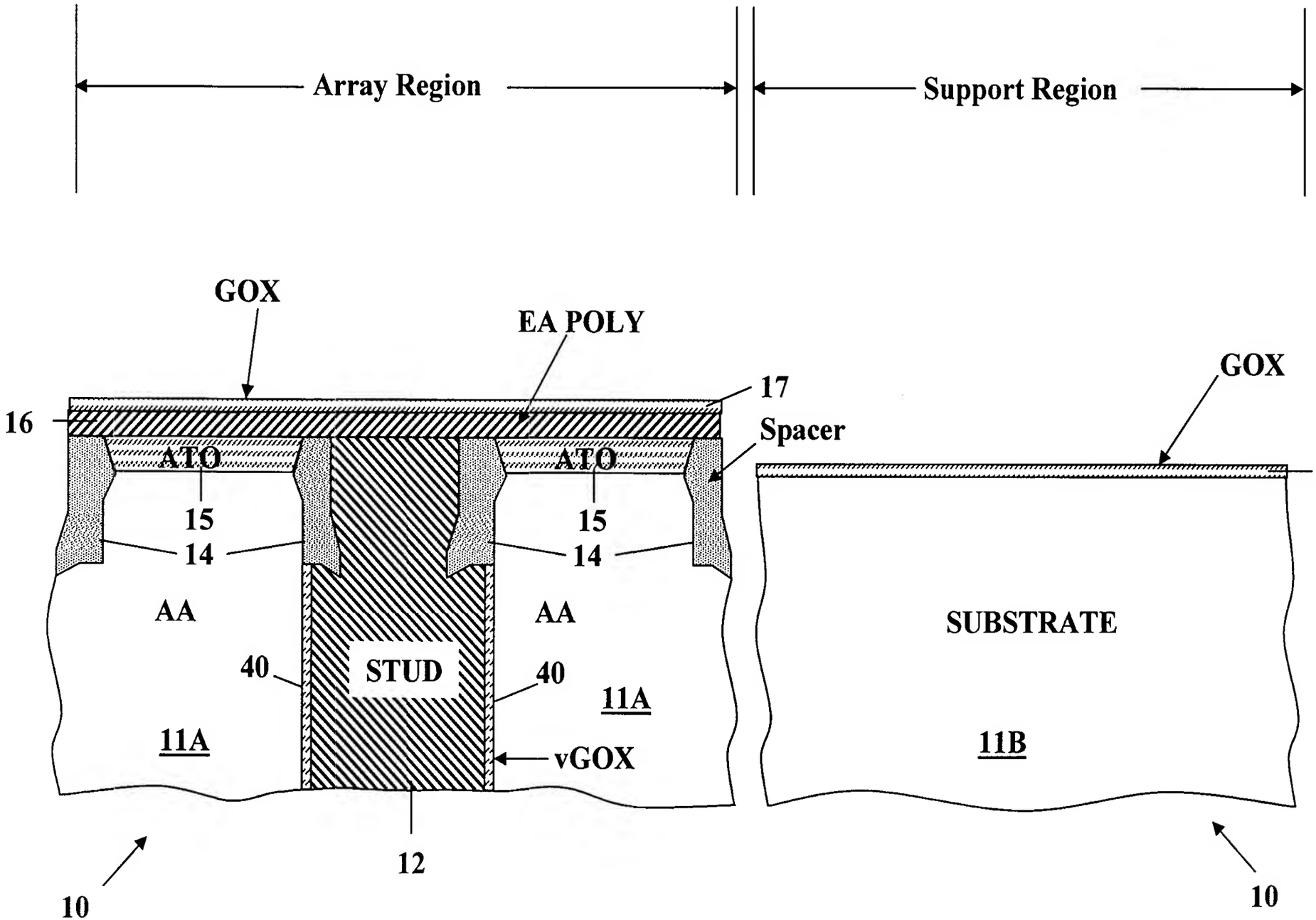


FIG. 5

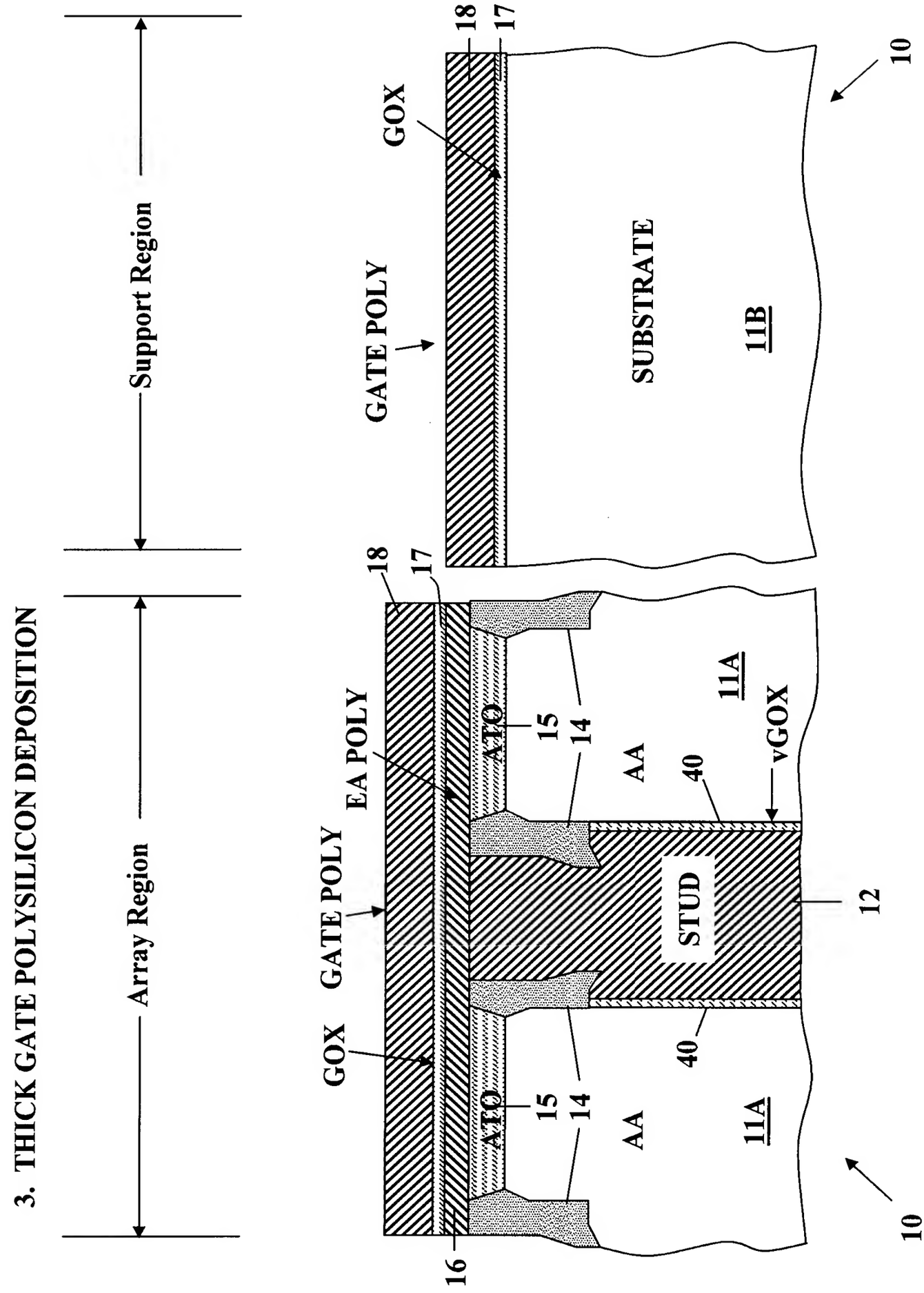

3. THICK GATE POLYSILICON DEPOSITION
Support Region
Array Region
GOX
GATE POLY
EA POLY
GATE POLY
GOX
18
17
ATO
15
14
AA
11A
40
vGOX
STUD
12
16
SUBSTRATE
11B
10

FIG. 6

4. BLOCKING MASK AT SUPPORT REGION

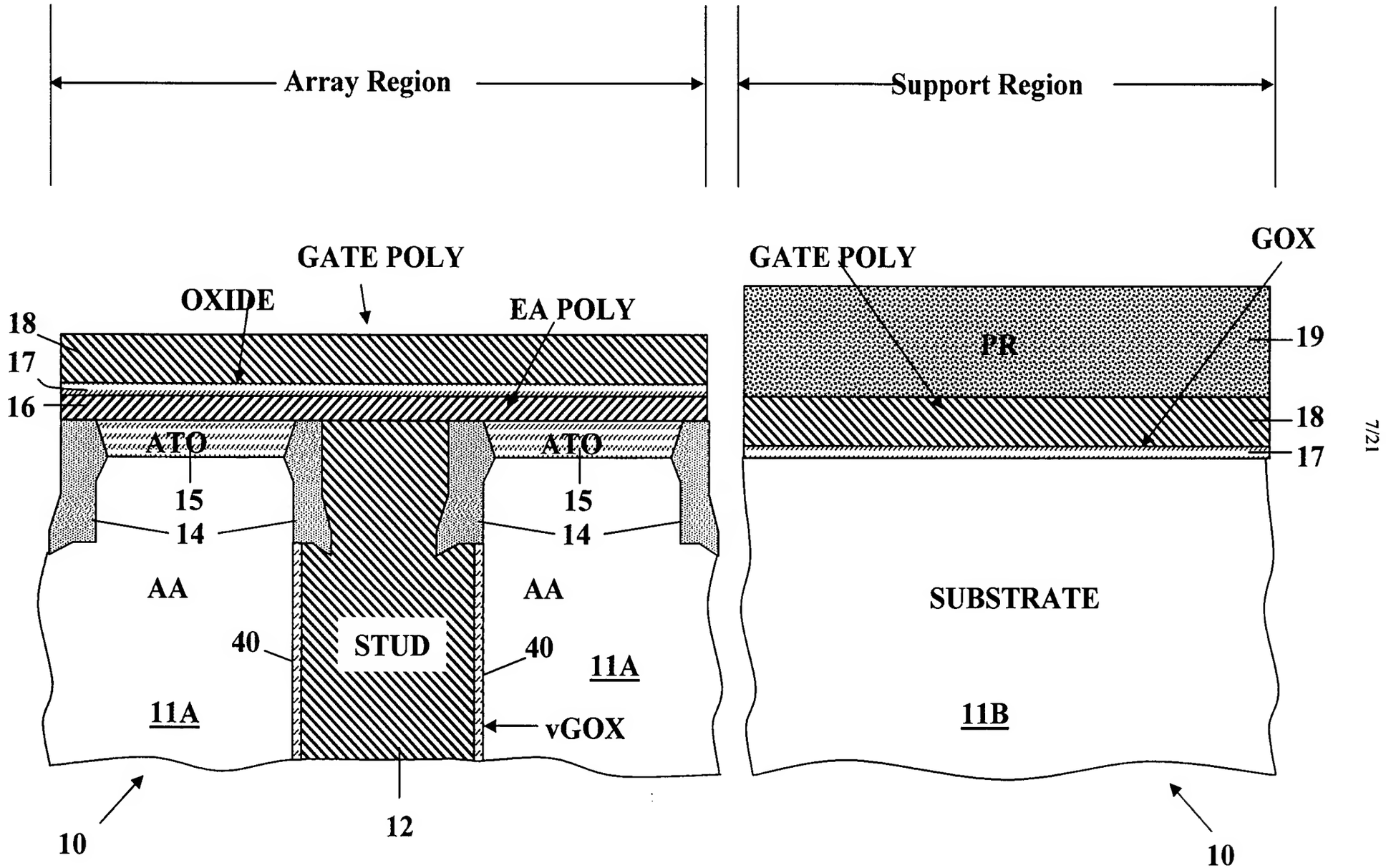


FIG. 7

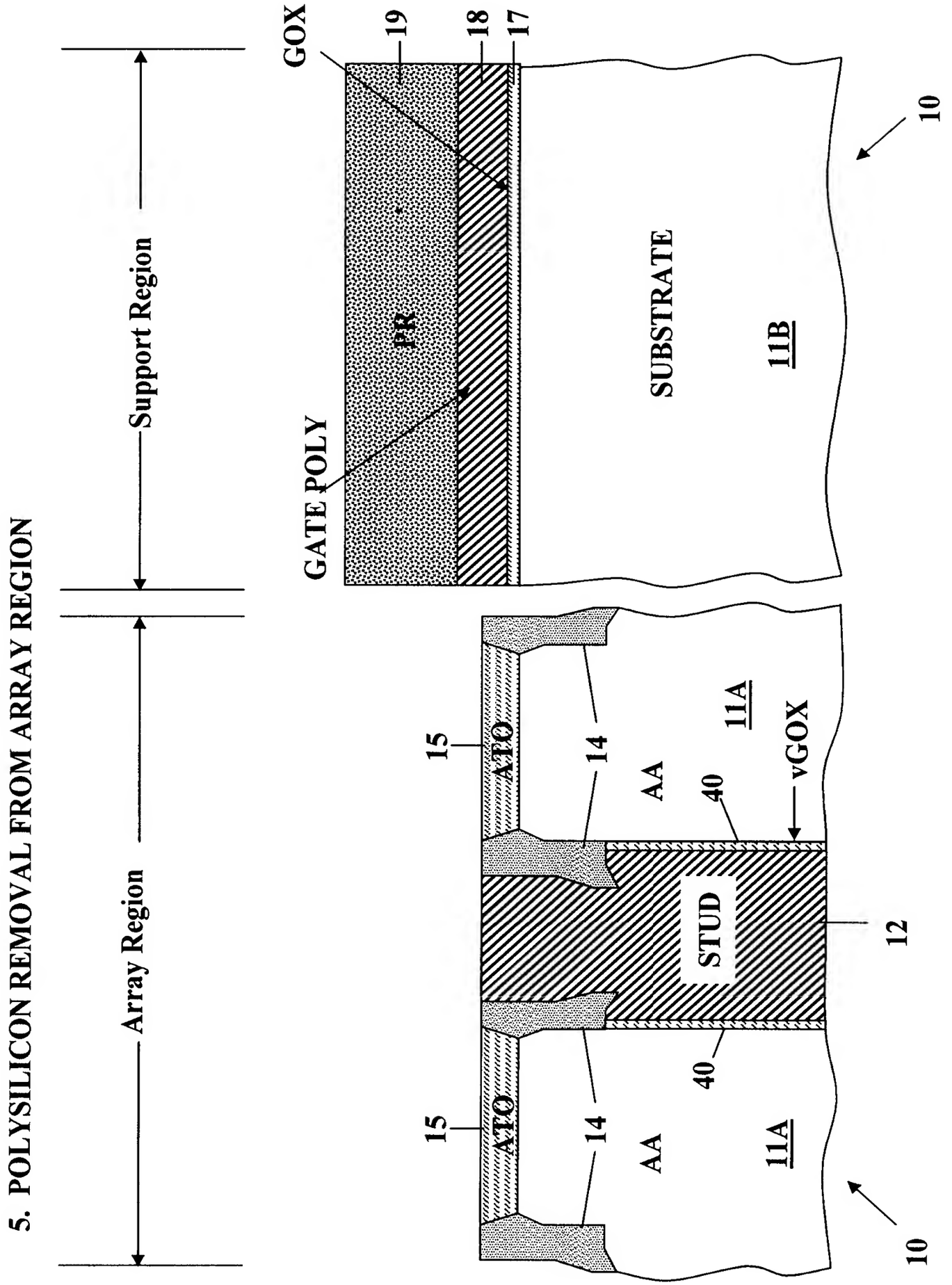

5. POLYSILICON REMOVAL FROM ARRAY REGION
Support Region
Array Region
GOX
19
18
17
GATE POLY
PR
SUBSTRATE
11B
10
15
ATO
14
AA
11A
40
vGOX
STUD
12
15
ATO
14
AA
40
11A
10

FIG. 8

6. PHOTORESIST STRIP

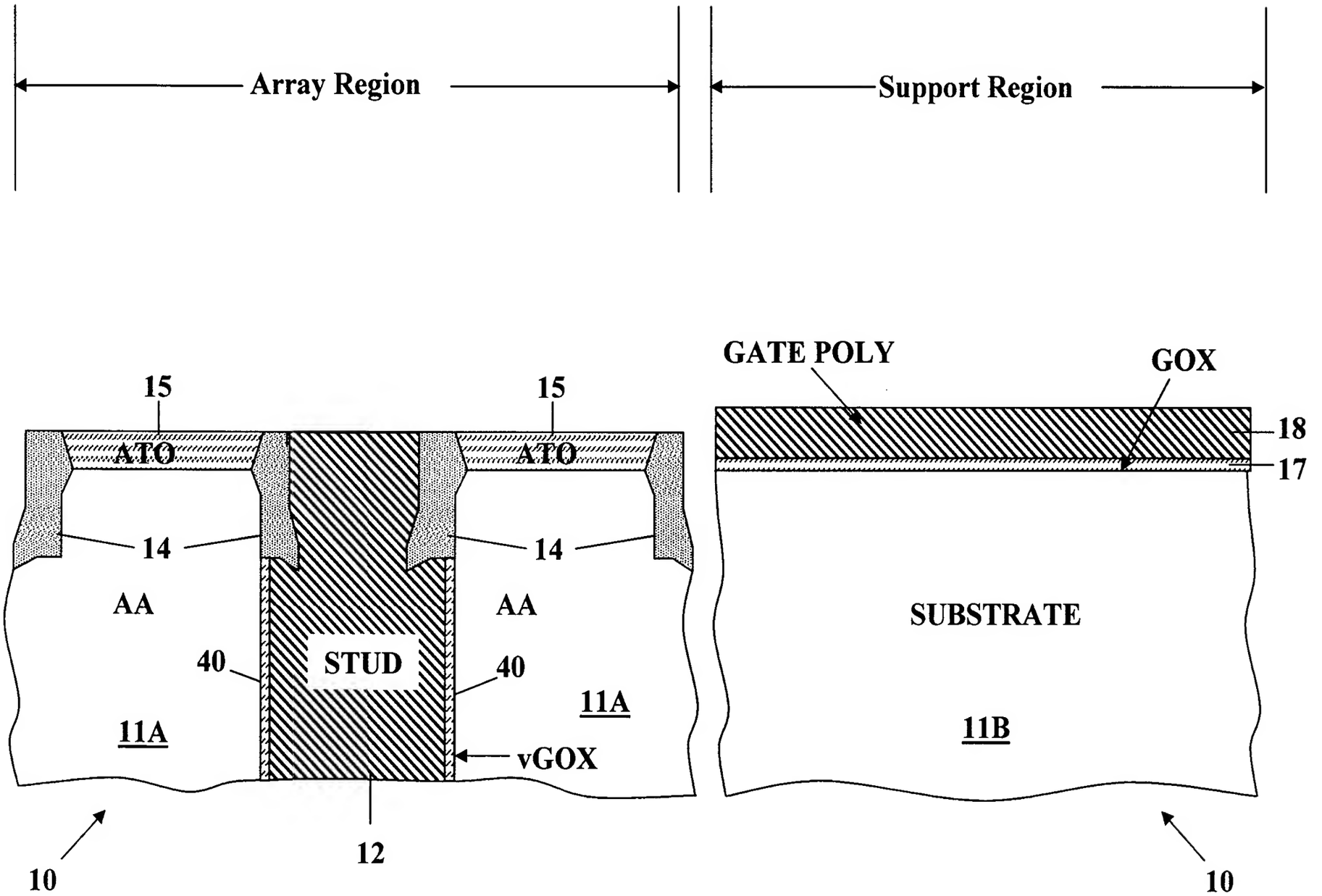


FIG. 9

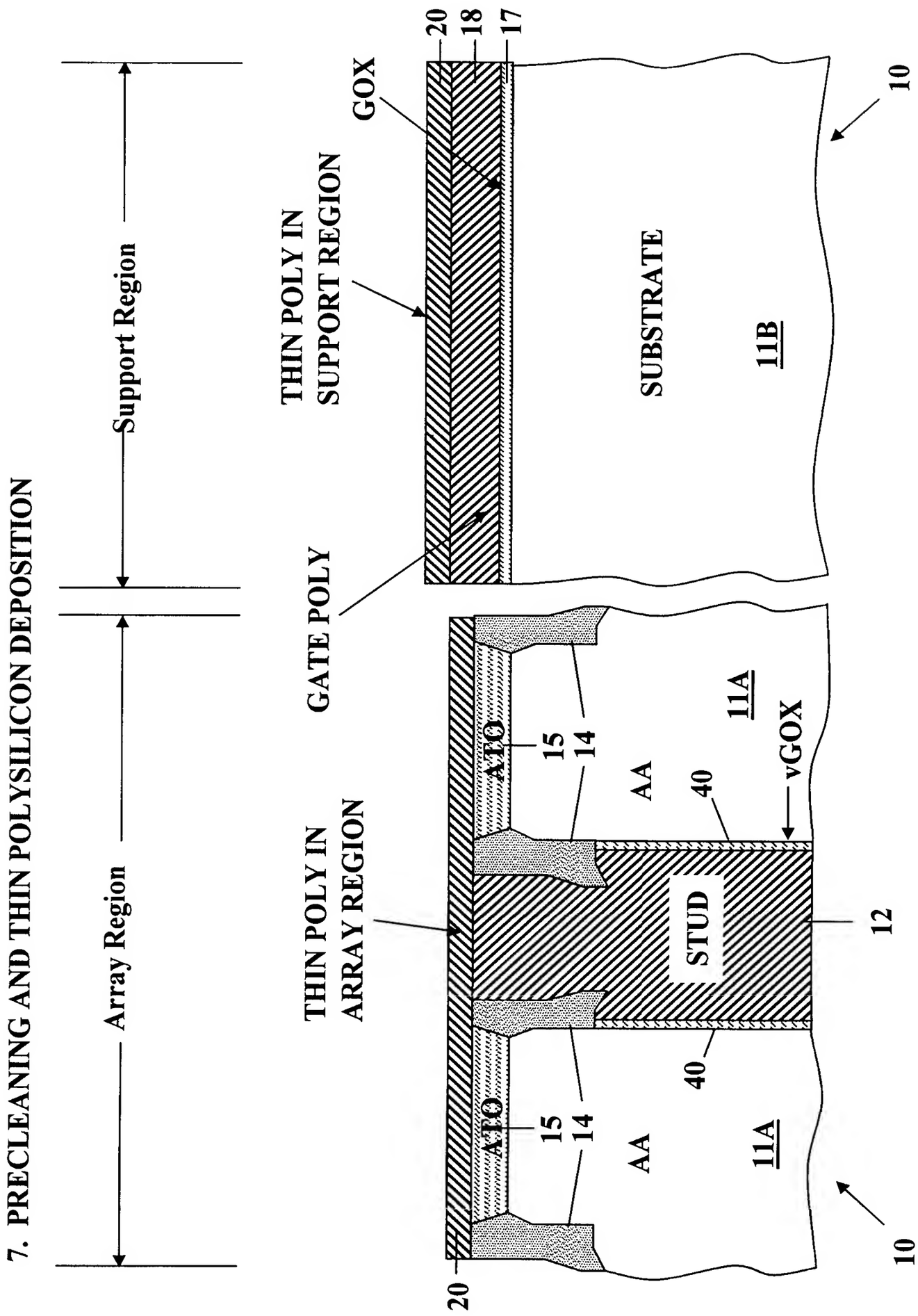

7. PRECLEANING AND THIN POLYSILICON DEPOSITION
Support Region
Array Region
THIN POLY IN SUPPORT REGION
GATE POLY
THIN POLY IN ARRAY REGION
GOX
20
18
17
10
SUBSTRATE
11B
11A
vGOX
ATO
15
14
AA
40
STUD
12
20
10

FIG. 10

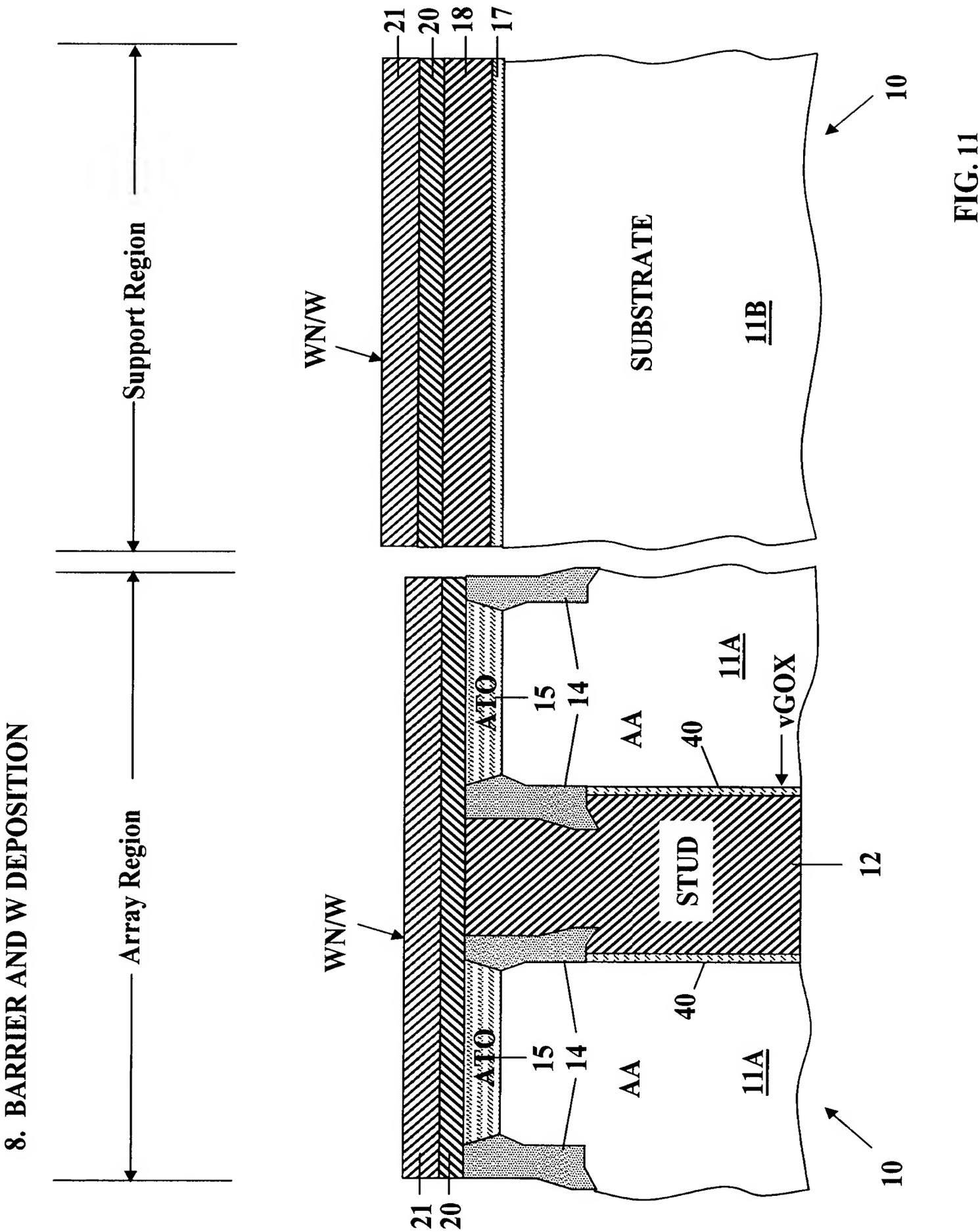

8. BARRIER AND W DEPOSITION
Support Region
Array Region
21
20
18
17
WN/W
SUBSTRATE
11B
10
ATO
15
14
AA
11A
40
vGOX
STUD
12
WN/W
ATO
15
14
AA
11A
40
21
20
10

FIG. 11

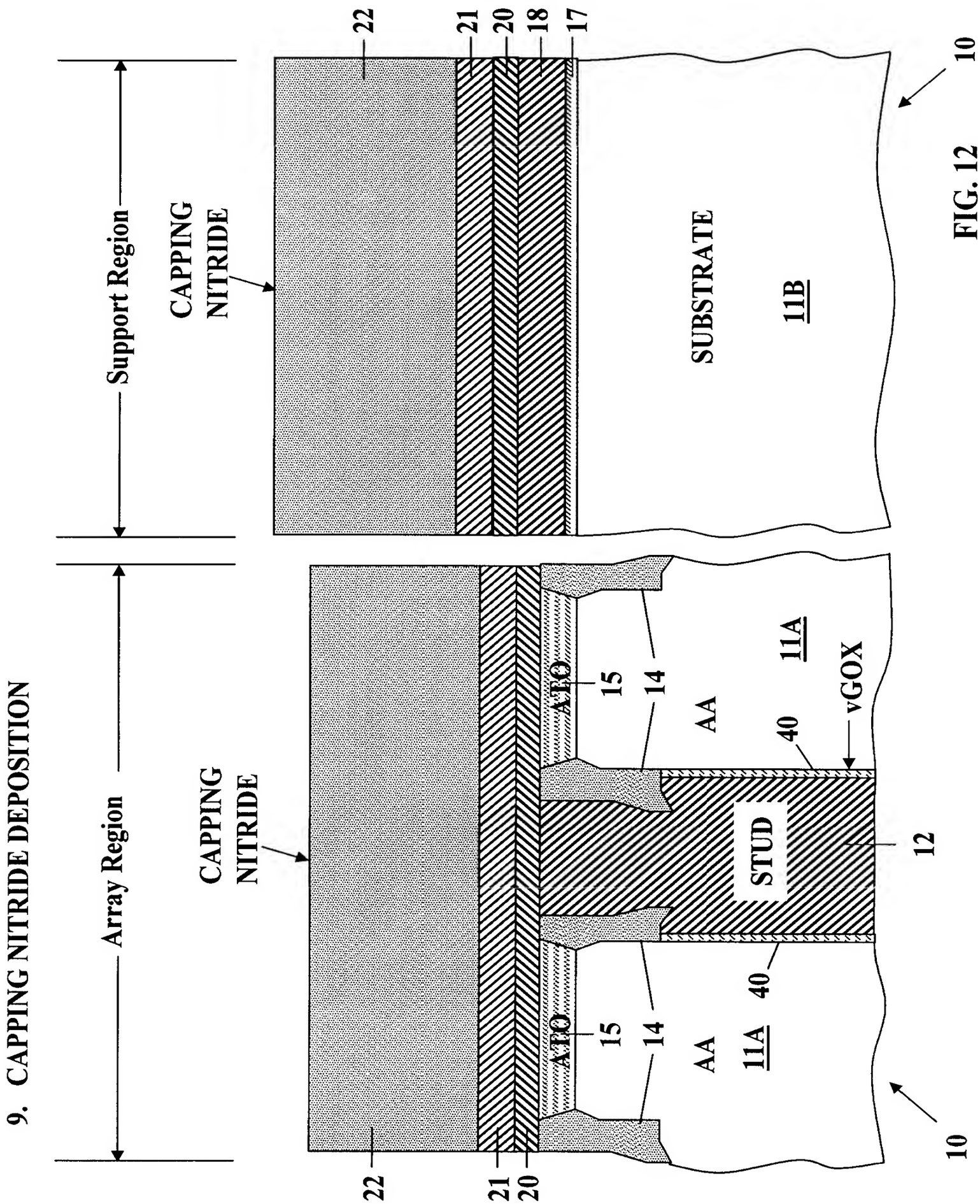

9. CAPPING NITRIDE DEPOSITION
Support Region
CAPPING NITRIDE
Array Region
CAPPING NITRIDE
22
21
20
18
17
SUBSTRATE
11B
10
ATO
15
14
AA
11A
vGOX
40
STUD
12
22
21
20
ATO
15
14
AA
11A
40
10

FIG. 12

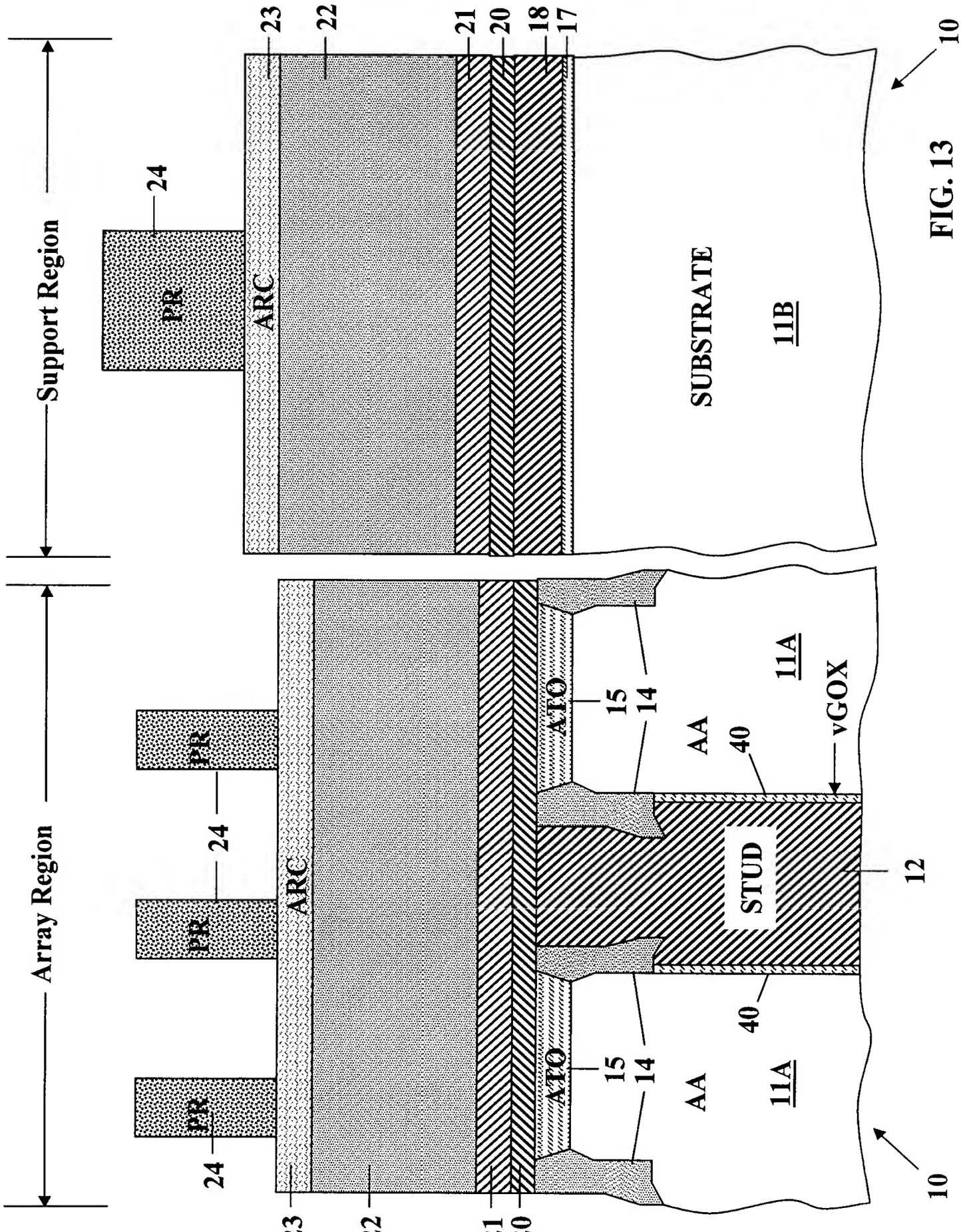

10. GATE PATTERNING
Array Region
Support Region
PR
ARC
24
23
22
21
20
18
17
SUBSTRATE
11B
10
ATO
15
14
AA
40
11A
vGOX
STUD
12

FIG. 13

11. HARD MASK OPEN

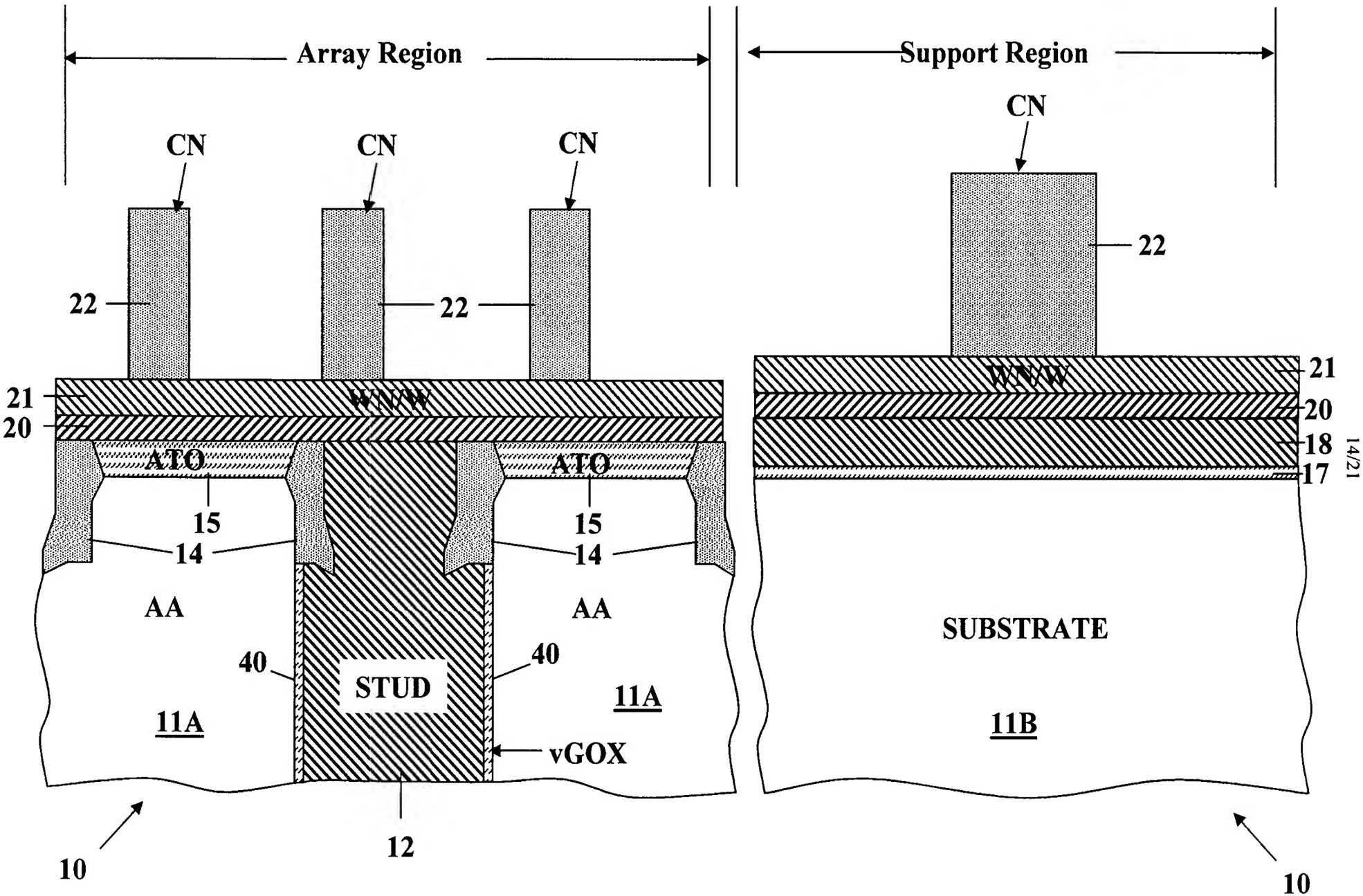


FIG. 14

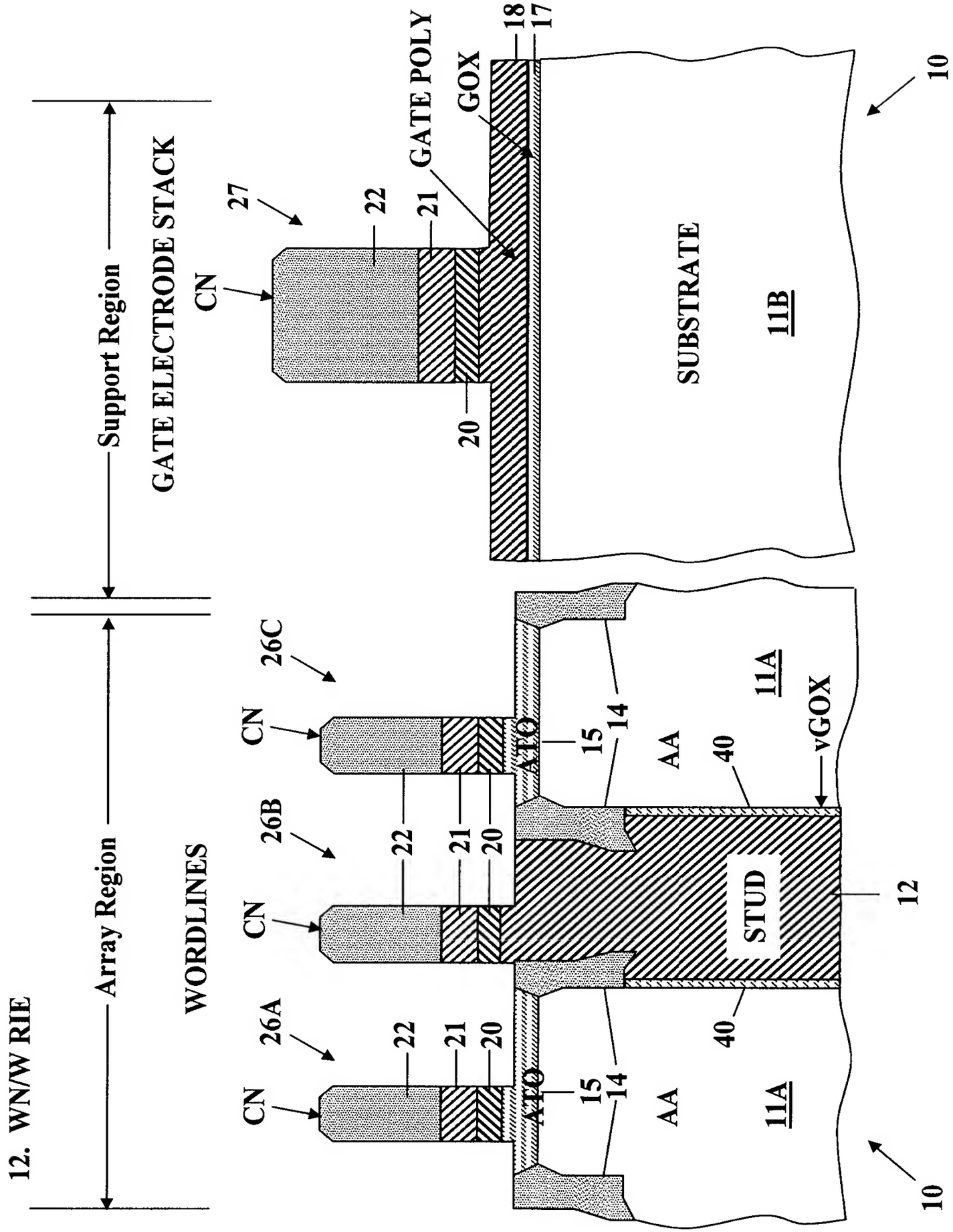

12. WN/W RIE
Array Region
WORDLINES
Support Region
GATE ELECTRODE STACK
CN
27
22
21
GATE POLY
GOX
18
17
20
SUBSTRATE
11B
10
26C
26B
26A
ATO
15
14
AA
40
11A
vGOX
STUD
12

FIG. 15

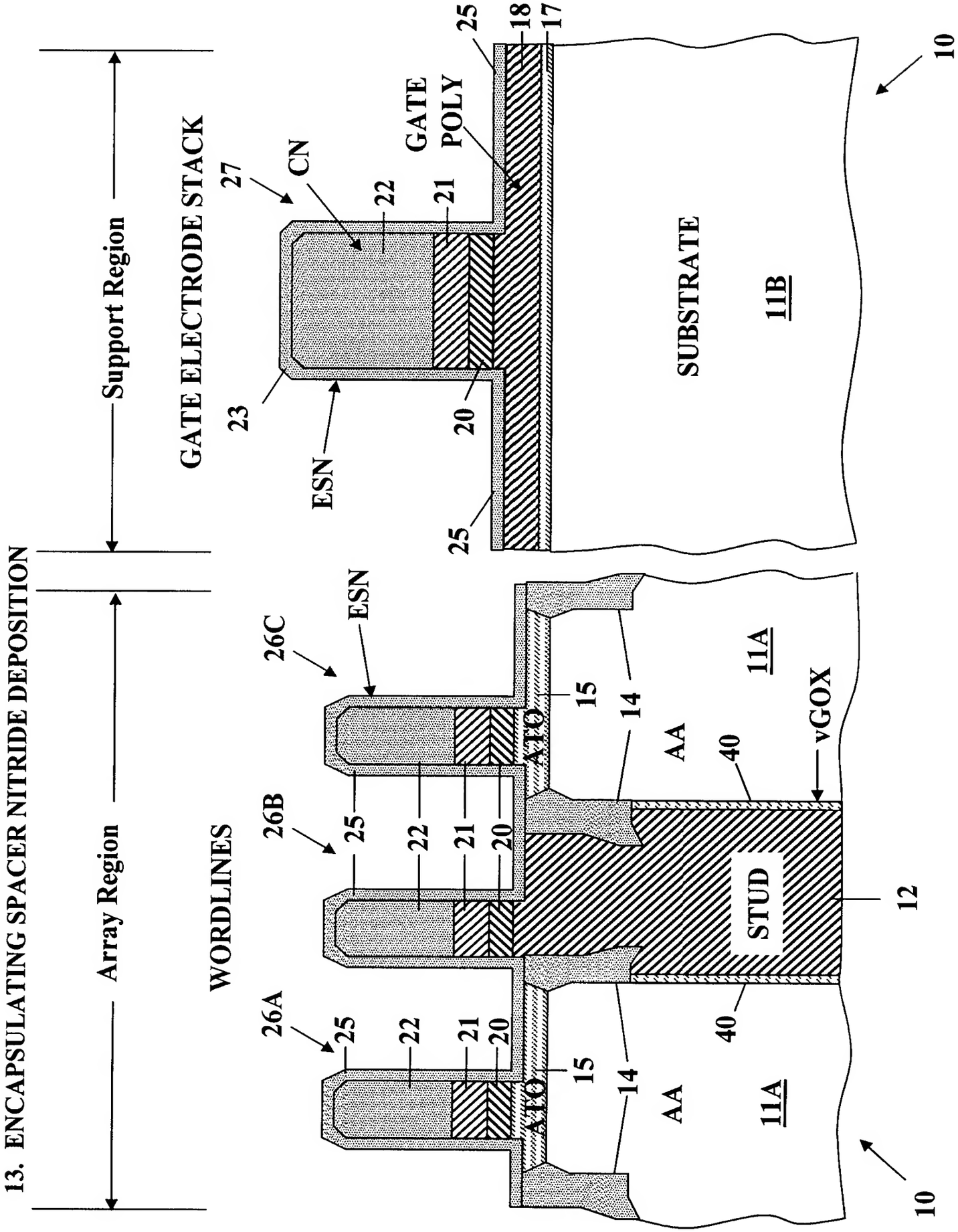

13. ENCAPSULATING SPACER NITRIDE DEPOSITION
Support Region
Array Region
GATE ELECTRODE STACK
WORDLINES
27
CN
22
21
GATE POLY
25
18
17
10
23
ESN
20
25
SUBSTRATE
11B
26C
ESN
15
14
ATO
AA
11A
40
vGOX
26B
25
22
21
20
STUD
12
26A
25
22
21
20
15
14
ATO
AA
40
11A
10

FIG. 16

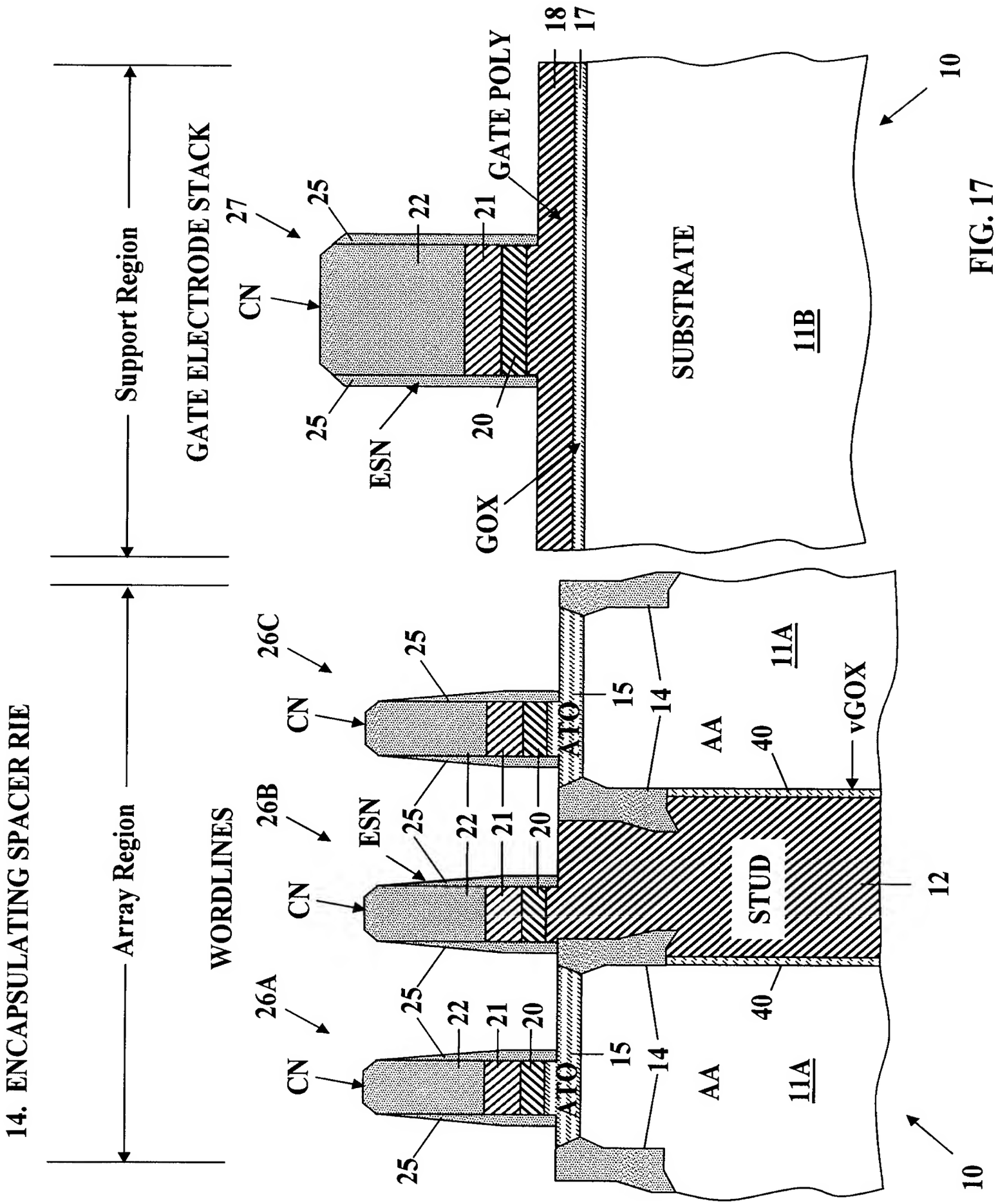

14. ENCAPSULATING SPACER RIE
Array Region
Support Region
WORDLINES
GATE ELECTRODE STACK
26A
26B
26C
CN
ESN
25
22
21
20
ATO
15
14
AA
11A
40
vGOX
STUD
12
10
27
GATE POLY
18
17
SUBSTRATE
11B
GOX

FIG. 17

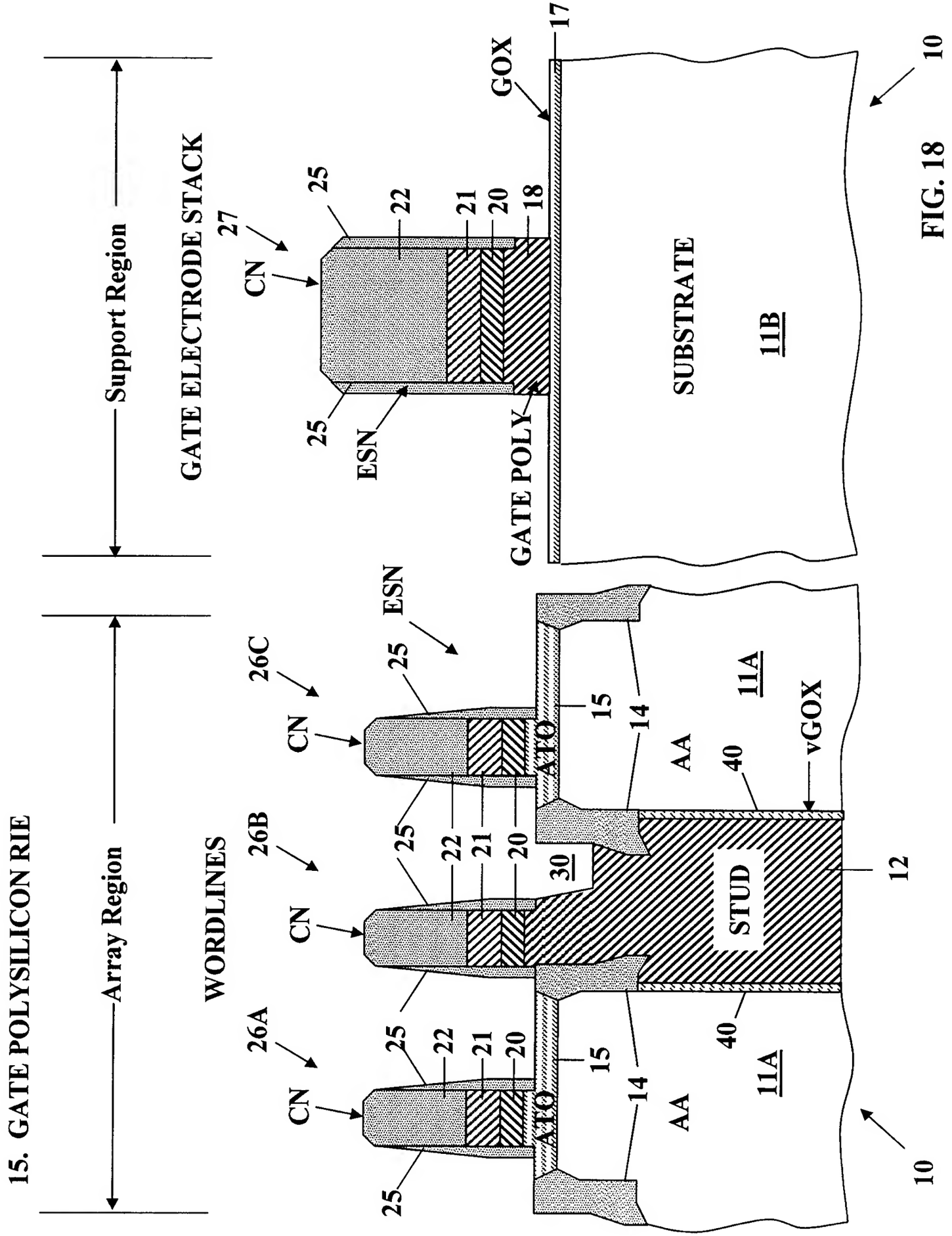
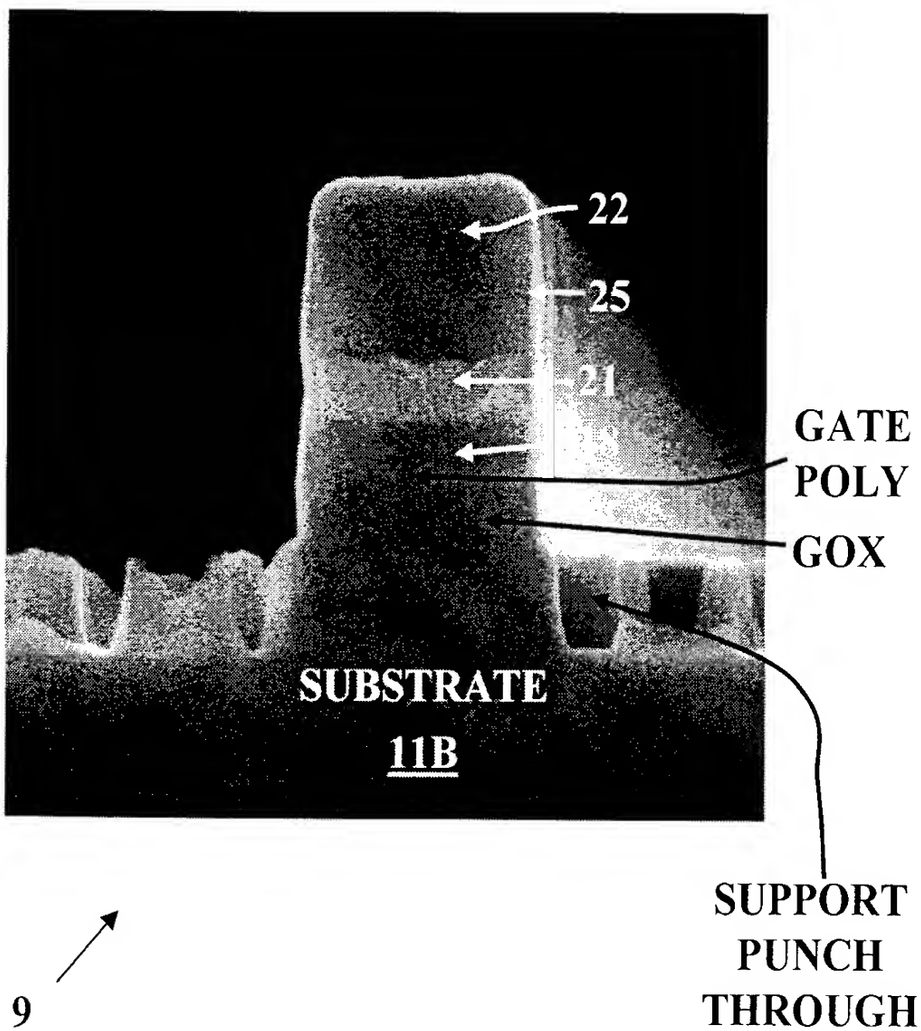

15. GATE POLYSILICON RIE
Array Region
Support Region
WORDLINES
GATE ELECTRODE STACK
26A
26B
26C
CN
25
22
21
20
ESN
ATO
15
14
AA
11A
40
vGOX
30
STUD
12
10
27
GOX
17
18
GATE POLY
SUBSTRATE
11B

FIG. 18

SUPPORT PUNCH THROUGH



PRIOR ART

FIG. 19A

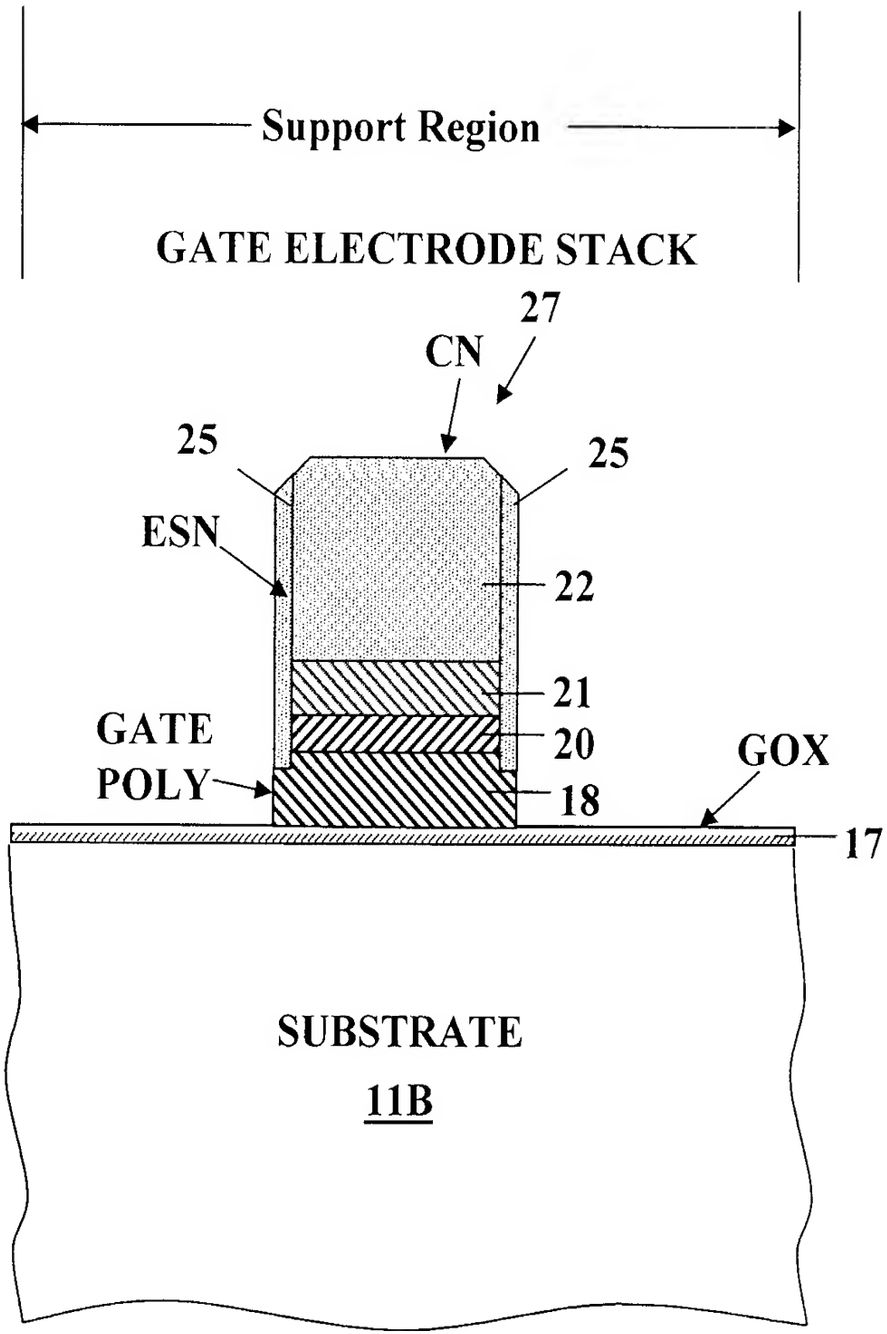
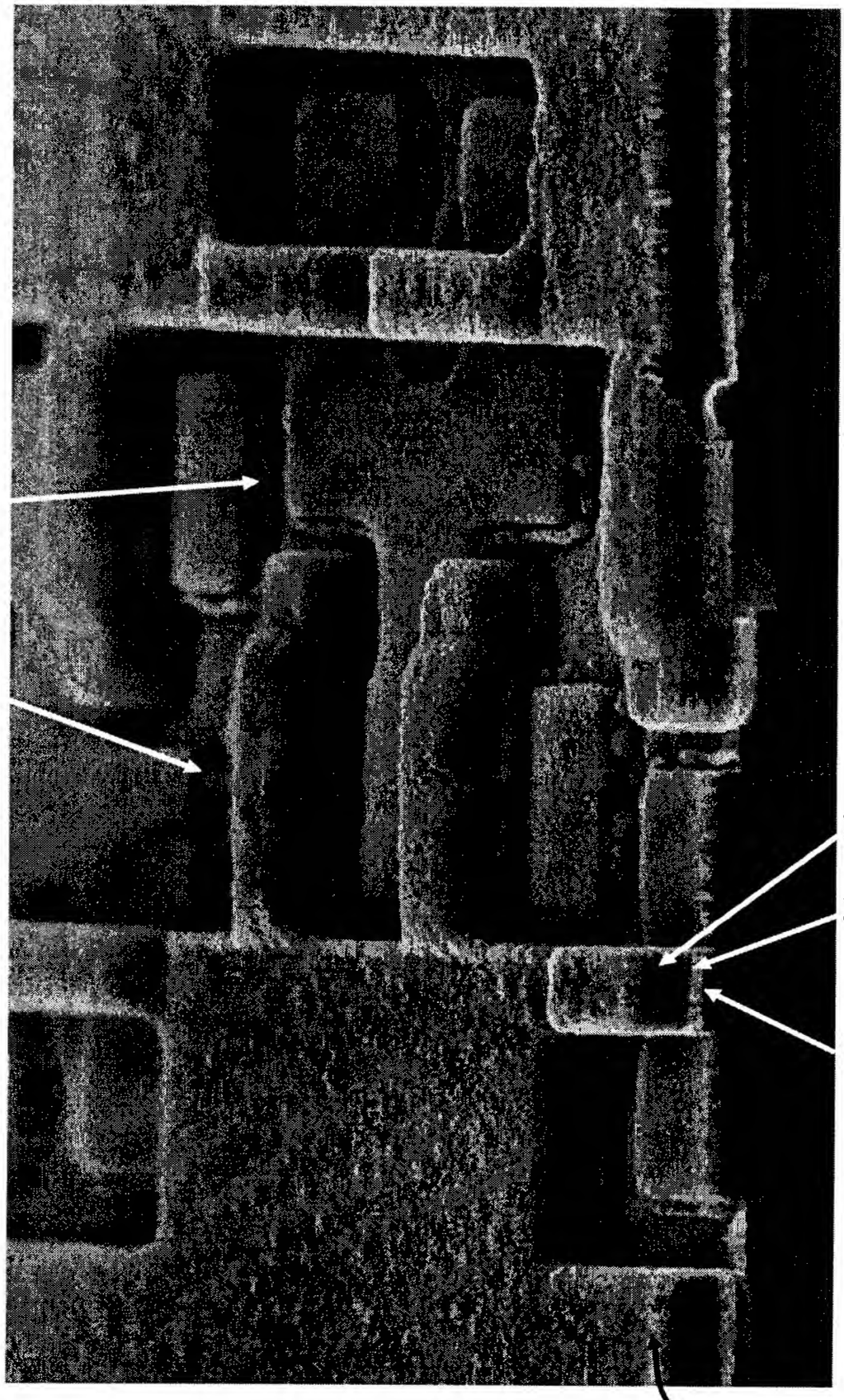


FIG. 19B

FIS920030421US1



PRIOR ART

FIG. 20

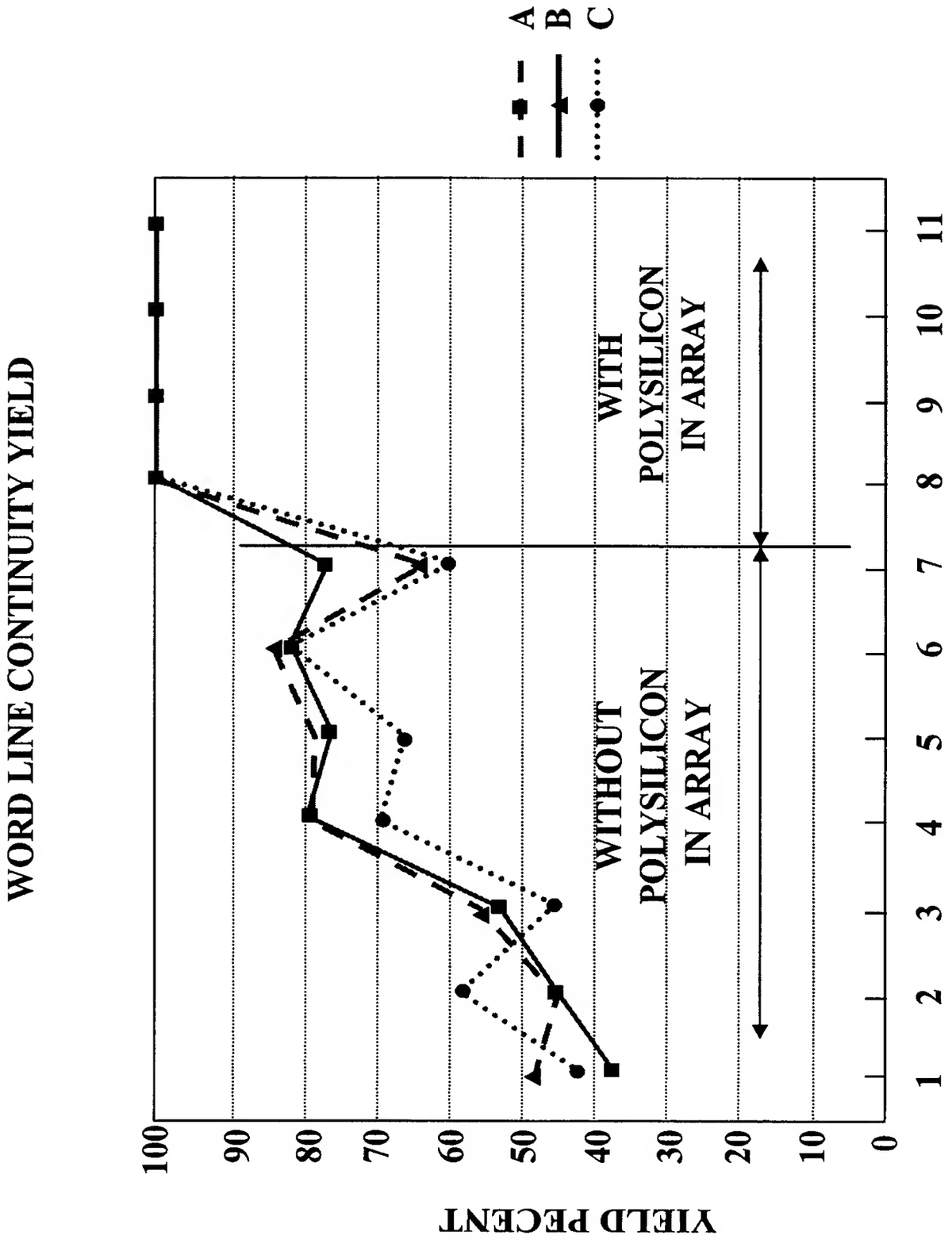

WORD LINE CONTINUITY YIELD
A
B
C
WITH POLYSILICON IN ARRAY
WITHOUT POLYSILICON IN ARRAY
YIELD PECENT
WAFER
100
90
80
70
60
50
40
30
20
10
0
1
2
3
4
5
6
7
8
9
10
11

FIG. 21